Ordering number: EN 2651B

Monolithic Linear IC

LA3246

Stereo Preamplifier for Compact Double Cassette Playback-only Use

Overview

The LA3246 is a stereo preamplifier IC for double cassette tape playback-only use. The LA3246 is intended for use in portable radio-cassette tape recorders and tape decks.

Applications

- Stereo compact cassette player for playback-only use
- Stereo cassette deck player

Functions

- Preamplifier × 2, Mixing amplifier × 1, Electronic switch × 6

Features

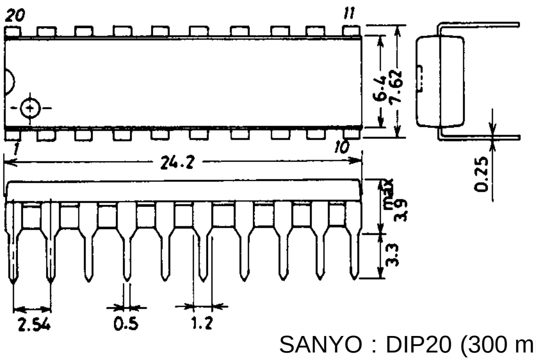
- On-chip electronic switch for input select (auto reverse or A deck/B deck select)
- On-chip electronic switch for normal/higher dubbing select and electronic switch for metal/normal tape select
- Wide operating voltage range (V_{CC} op = 3.5 to 14 V)
- With output MIX pin (for music select control)
- Low noise voltage range (V_{NI} = 0.9 µV typ, Rg = 2.2 kΩ NAB)
- Can be used in conjunction with the LA3240, 3241, 3242 to easily make up a doublecassette dubbing system.

Package Dimensions

unit : mm

3021B-DIP20

[LA3246]



SANYO : DIP20 (300 mil)

Specifications

Maximum Ratings at Ta = 25°C

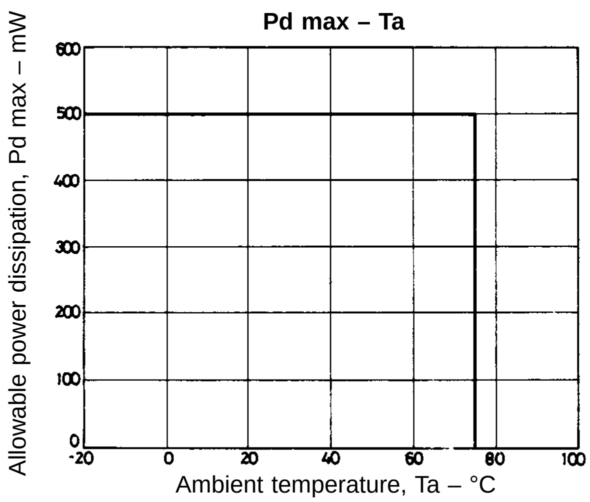
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		16	V
Allowable power dissipation	Pd max		500	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Maxiumum Ratings at Ta = 25°C

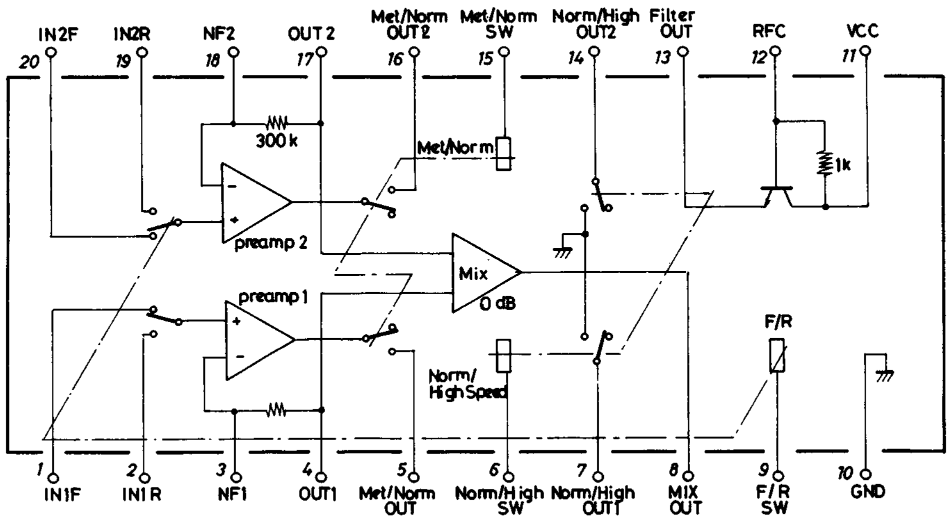
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		6	V
Operating voltage range	V_{CC} op		3.5 to 14	V

Operating Characteristics at Ta = 25°C, V_{CC} = 6.0 V, R_L = 10 kΩ, f = 1 kHz, 0 dB = 0.775 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	Icco	Nor/Nor speed forward	5	7	12	mA
	Iccs	Metal/High speed forward	7	10	17	mA
Voltage gain (Open)	VGo		75	85		dB
Voltage gain (Closed)	VG	Nor/Nor speed, NAB	39.5	40.5	41.5	dB
Total harmonic distortion	THD	V_O = 0.65 V, Nor/Nor speed		0.03	0.2	%
Maximum output voltage	V_O max	THD = 1%, Nor/Nor speed	0.7	1.2		V
Crosstalk (between channels)	CT1	V_O = –5 dBm, Rg = 2.2 kΩ, Nor/Nor speed	50	65		dB
Crosstalk (between F/R)	CT2	V_O = –5 dBm, Rg = 2.2 kΩ, Nor/Nor speed	50	65		dB
Channel balance	V_{BL}	V_{IN} = –50 dBm		0	2	dB
Equivalent input noise voltage	V_{NI}	Rg = 2.2 kΩ, B.P.F 20 Hz to 20 kHz, Nor/Nor speed		0.9	1.7	µV
MIX output voltage	V_OMIX	V_O1, V_O2 = 0 dBm	–3	0	+3	dB
Ripple filter output current	$I_{F\ OUT}$			10	15	mA
Electronic switch ON-state resistance	Ron	Between P1 to P4 and 5, between pin 16 and 17		100	250	Ω
		Between P1 to P7 and 10, between pin 10 and 14		30	70	Ω
DC feedback resistance	R_F		240	300	360	Ω
Input bias current	I_F			0.5	3.0	µA

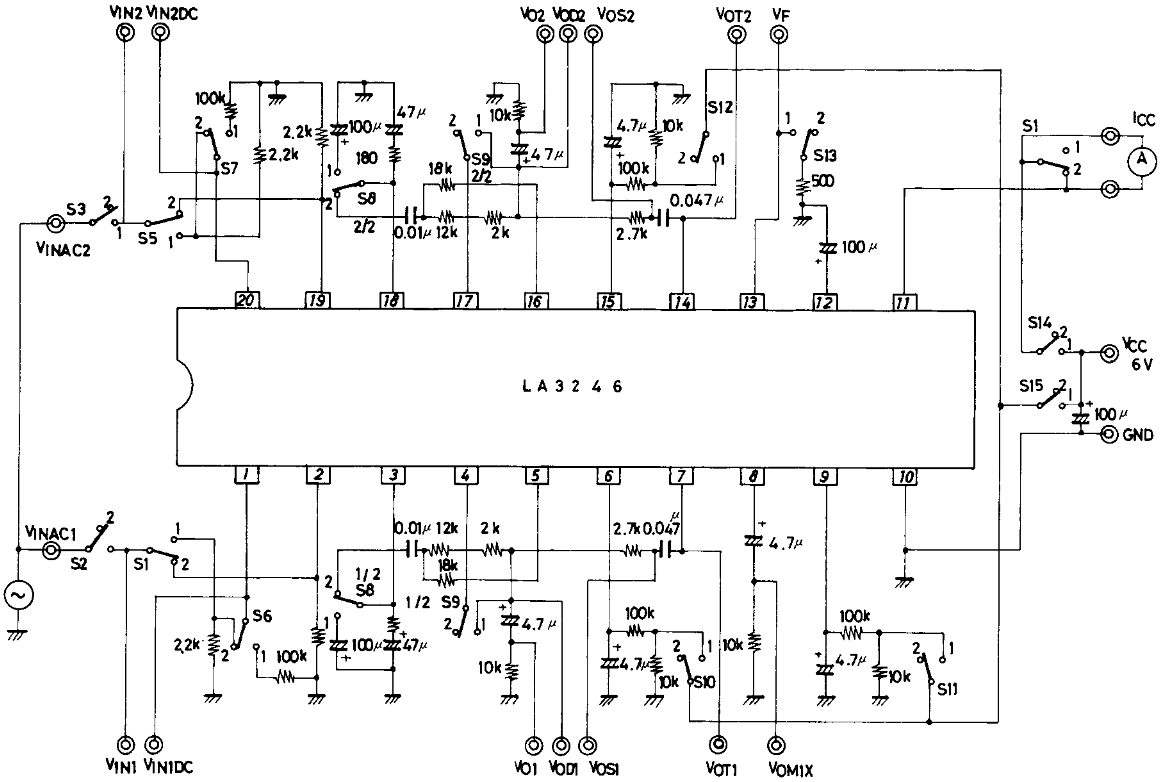


Equivalent Circuit Block Diagram

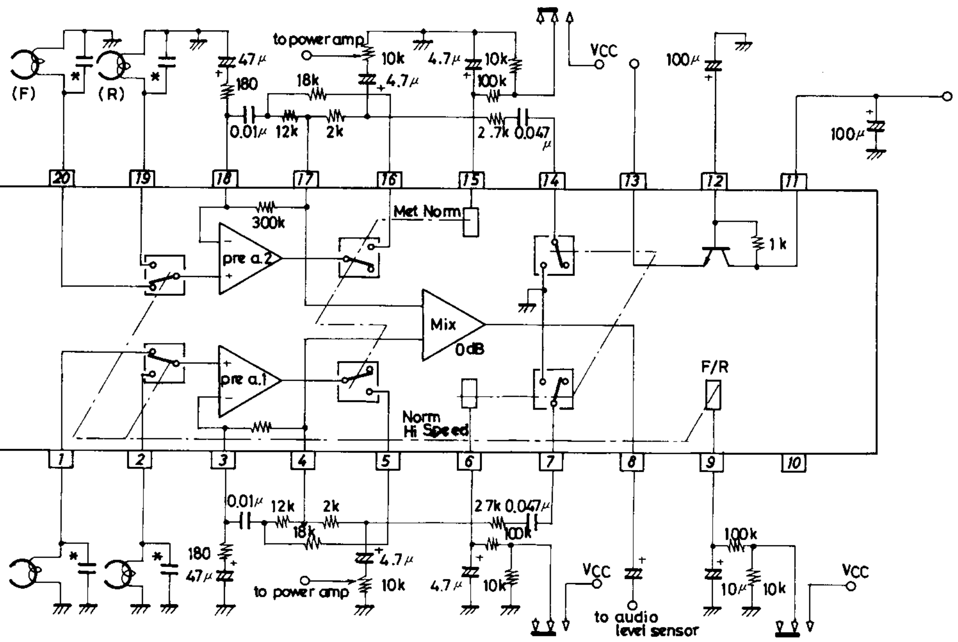


Top view

Test Circuit



Sample Application Circuit



Unit (resistance: Ω, capacitance: F)

Note 1. The output frequency characteristic for Nor Tape/High speed mode (pin 6: High, pin 15: Low) and that for Metal Tape/Nor speed mode (pin 6: Low, pin 15: Low) are set to be the same.

2. Since the input bias current flows out of pins 1, 2 and pins 19, 20, a resistor (recommended value: 30 kΩ to 350 kΩ, maximum value: 500 kΩ) must be connected a coupling capacitor in series with these pins.

3. *: A capacitor must be connected to the input to absorb a surge.

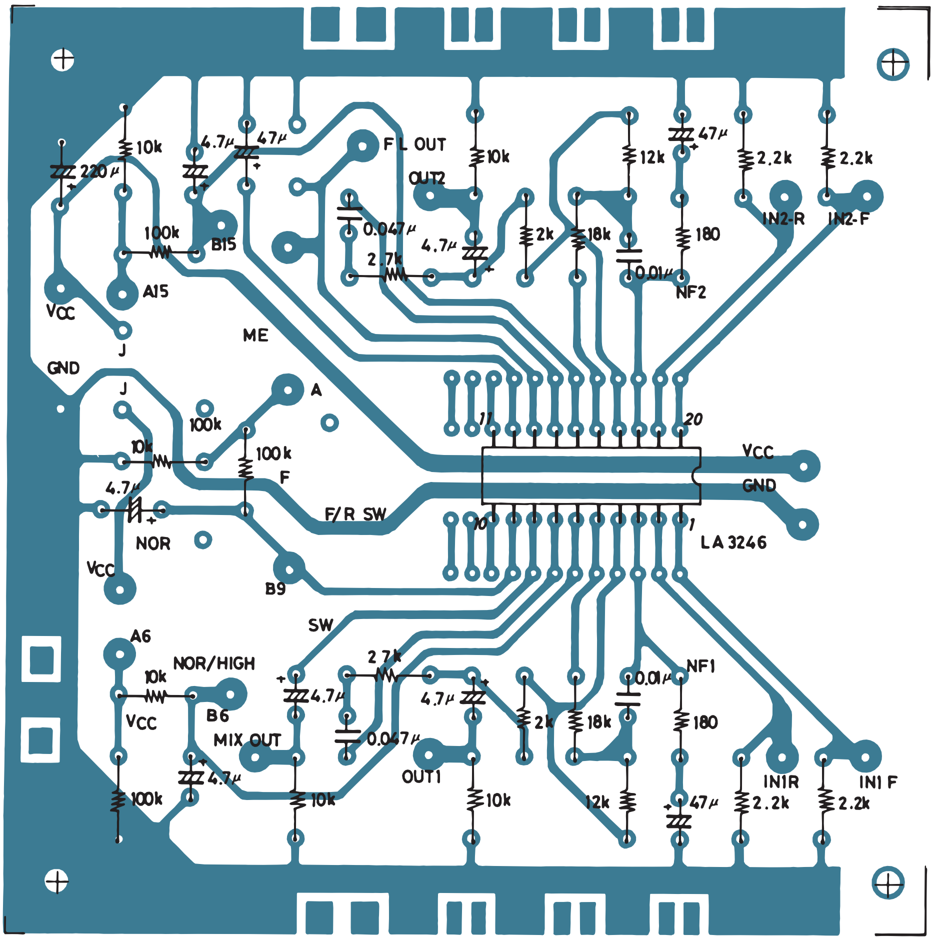
4. The electronic select switching level is approximately $1/2 \times (V_{CC}–0.9)$.

5. The value of the capacitor connected to pin 12 can be increased/decreased to adjust starting time t_s at the time of application of V_{CC}. (C = 100 µF, t_s = 0.4 s.) If the capacitor value is made less than 47 µF, the ripple rejection will get worse.

6. No capacitor is connected to pin 13. (Even if connected, the ripple can not be rejected.)

7. Extreme caution should be exercised when handling the IC as it is subject to dielectric breakdown.

Sample Printed Circuit Pattern (Cu-foiled area)



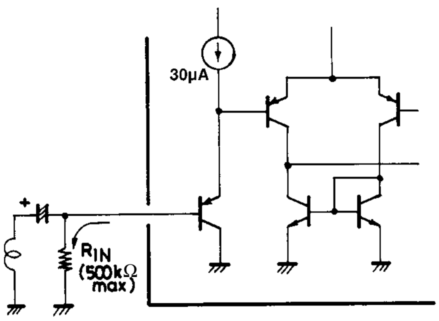
115×115 mm²

Unit (resistance: Ω, capacitance: F)

IC Usage Notes

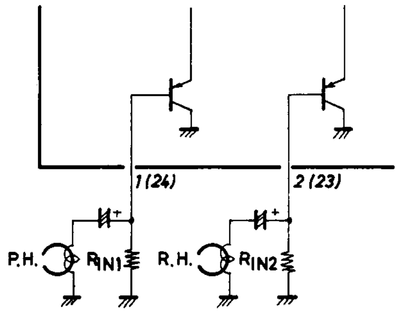
(1) It is recommended to connect a surge absorbing capacitor across input pins 1, 2 and GND and across input pins 19, 20 and GND.

(2) The base of a PNP transistor is connected to input pins 1, 2 and 19, 20. If an electrolytic capacitor is connected in series with the input pins, connect input resistor R_{IN} must not exceed 500 kΩ. (Reason: To minimize the variation in output DC voltage at the time of input switching)



If a resistor of more than 500 kΩ is connected across input pin and GND, the noise (output) caused by amp 1 and amp 2 select is liable to increase at the time of F/R switching.

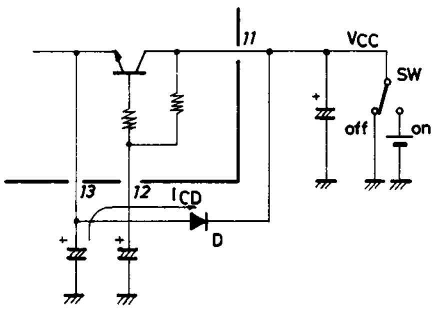
(3) When an electrolytic capacitor is connected to input pins 1, 2 (or 23, 24), make the value of $R_{IN}1$ as equal to that of $R_{IN}2$ as possible.



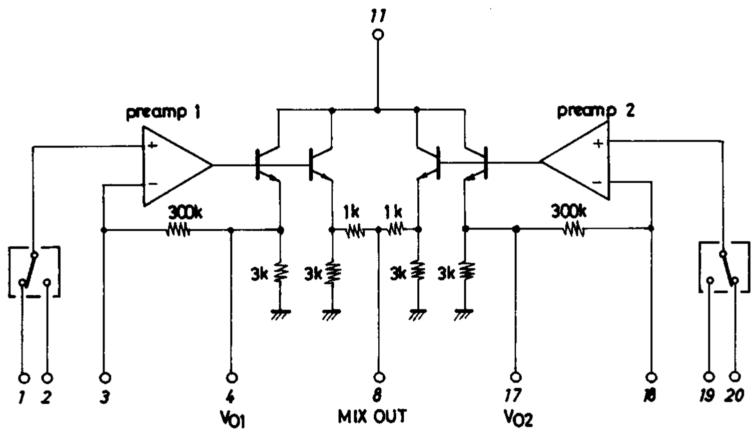
The difference in the value between $R_{IN}1$ and $R_{IN}2$ causes the variation in amp output DC voltage at the time of F/R switching. Therefore, the input DC voltage (voltage across R_{IN}) must be made as equal as possible.

(4) The amplifier output characteristics are designed to be the same in the Nor Tape/High Speed (pin 15 GND/pin 6 V_{CC}) and Me Tape/Nor Speed (pin 15 V_{CC}/pin 6 GND) modes. (Refer to sample application circuit, external constants.)

(5) When externally turning ON/OFF power supply pin 11 (by bringing pin 11 to $+V_{CC}$/GND level) with a capacitor connected to pin 13, connect external diode D, as shown below, so that no breakdown (or deterioration) of the IC system is caused by I_{CD} when the switch is turned OFF. When no capacitor is connected to pin 13, diode D is not required.



(6) The output MIX circuit is of the emitter follower configuration as shown below.



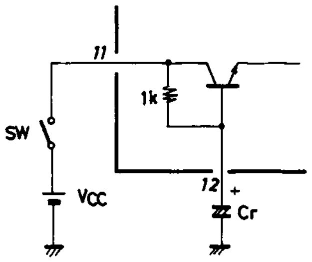
Unit (resistance: Ω)

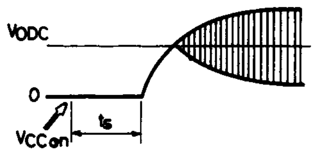
The MIX OUT output level V_O MIX at the time a signal is applied to preamp1 (or preamp2) only is 1/2 as compared with output levels V_O1, V_O2 at the time the same input signal is applied to both channels.

V_O MIX = 1/2 V_O1(= 1/2 × V_O2)

where $V_O1 = V_O2$

(7) Output waveform starting time





Example of rise waveform at pin 4 (or 17)

When supply voltage V_{CC} is switched ON, the amplifier output (pins 4, 17) will rise. Output waveform ON time t_s can be varied by capacitor Cr connected to pin 12.

Refer to Data Cr – t_s.

The minimum value of Cr is 47 μF.

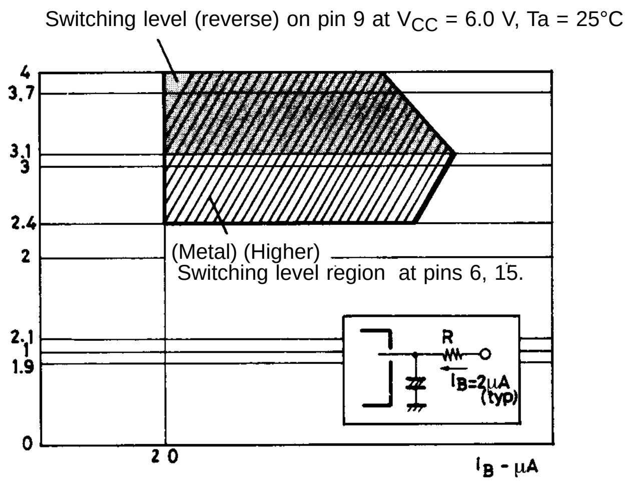
(8) Electronic select switching level

• The switch level at V_{CC} = 6.0 V is shown below.

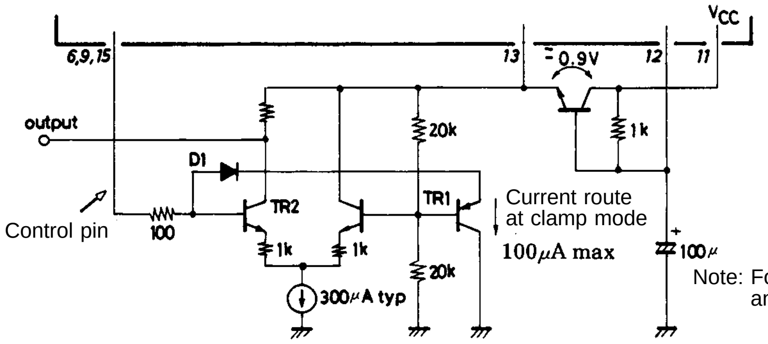
Pin	Switch Mode	Switching Level		Clamp Voltage	Control Current typ (flow-in) (at operation finish)	Mode	
		Operation Start	Operation Finish			(+)	(–)
6	Normal/Metal	2.1 V	2.4 V	3.7 V	2 μA	Metal	Normal
9	Forward/Reverse	2.1 V	3.1 V	3.4 V	2 μA	Reverse	Forward
15	Normal/Higher	2.1 V	2.4 V	3.7 V	2 μA	Higher	Normal

As shown above, there is a difference in the switching level at three control pins (6, 9, 15) between operation start and operation finish.

• Switching level and mode at each pin (experimental value)



- Control circuit
  The control circuit for each CONT pin is configured as shown below. When a voltage more than a given value is applied, the level on the pin is fixed by clamp diode D1.



Note: For D1, a Schottky diode is used for pin 9 and a silicon diode is used for pins 6, 15.

Unit (resistance: Ω, capacitance: F)

Description

- Switching level V_{SW} of the control circuit is fixed by voltage V13 which is 1/2 of the voltage on pin 13.

  V_{SW} = 1/2 V13

- Clamp voltage V_{CLP} at the time a voltage is applied to the CONT pin

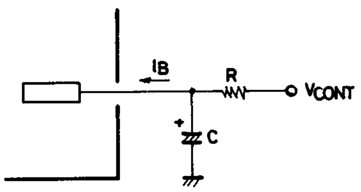
  $V_{CLP} = 1/2 \times V13 + V_D1 + V_{BE}1$
  $= 1/2 \times V13 + 0.6\ (0.3) + 0.6$
  $= 1/2 \times V13 + (0.9 \text{ or } 1.2)$

  where 0.9 V is for pin 9.
  1.2 V is for pins 6, 15.

- The maximum voltage at which the CONT pin is brought to GND level is fixed by the level at which the Q2 is completely turned OFF.
  This level is:
  $1/2 \times V13 - V_{BE}2 = 1/2 \times V13 - 0.6$ [V]

  Switching is performed at a level less than this.

- To turn ON/OFF
  When turning ON:



To turn ON the control circuit to finish the operation, I_B is required. Control voltage V_{OUT} is obtained with I_B of 4 μA min.

- V_{CONT} min = R × I_B max + Operation finish voltage.
  I_B = 4 μA
  Operation finish voltage
  Pins 6, 15 : = 1/2 × V13
  Pin 9 : = 1/2 × V13 + V_{BE}
  = 1/2 × V13 + 0.6 [V]
- V_{CONT} max = R × I_B max + Clamp voltage
  R is restricted by I_B max.

When the supply voltage is fixed, clamp voltage V_{CLP} is fixed. When resistor R is fixed based on a balance with capacitor C, resistor R is restricted by V_{CONT} max. as shown below.

$$I_B \text{ max} = 100\ \mu A \geqq \frac{V_{CONT} \text{ max} - V_{CLP}}{R}$$

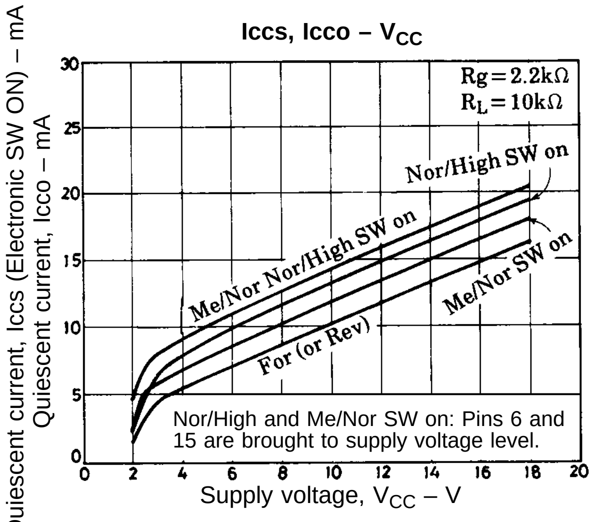
The minimum value of resistor R is fixed by this equation.
Example
Assuming V_{CC} = 10 V, V_{CONT} max = 10 V, Rmin is 50 kΩ.
Therefore, R = 100 kΩ presents no problem.

When turning OFF:
Bring the level on the CONT pin to a level less than:
$1/2 \times V13 - V_{BE}2 = 1/2 \times V13 - 0.6$ [V]

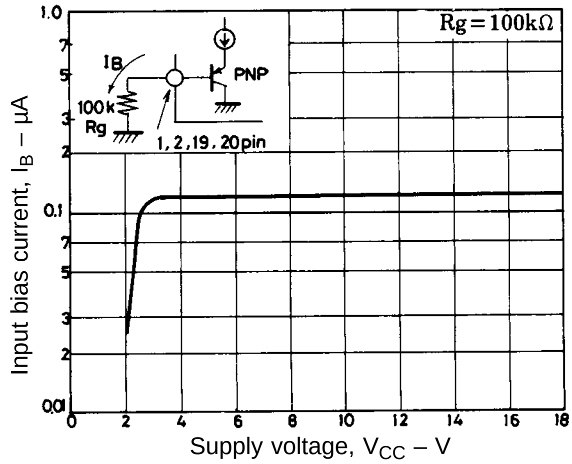
(9) Example of voltage on each pin

Rg = 2.2 kΩ, Ta = 25°C, V_{IN} = 0, pins 6, 9 and 15 = GND					
Pin	Supply voltage, V_{CC} – V				Unit
	4.5 V	6.0 V	9.0 V	12.0 V	
1	0.3	0.3	0.3	0.3	mV
2	0.3	0.3	0.3	0.3	mV
3	0.59	0.58	0.57	0.56	V
4	1.63	2.23	3.65	5.02	V
5	1.63	2.23	3.65	5.02	V
6	(GND) 0	(GND) 0	(GND) 0	(GND) 0	V
7	0	0	0	0	V
8	1.63	2.29	3.64	5.01	V
9	(GND) 0	(GND) 0	(GND) 0	(GND) 0	V
10	(GND) 0	(GND) 0	(GND) 0	(GND) 0	V
11	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V
12	4.48	5.96	8.97	11.23	V
13	3.72	5.20	8.21	11.98	V
14	0	0	0	0	V
15	(GND) 0	(GND) 0	(GND) 0	(GND) 0	V
16	1.63	2.23	3.65	5.02	V
17	1.63	2.23	3.65	5.02	V
18	0.59	0.58	0.57	0.56	V
19	0.3	0.3	0.3	0.3	mV
20	0.3	0.3	0.3	0.3	mV

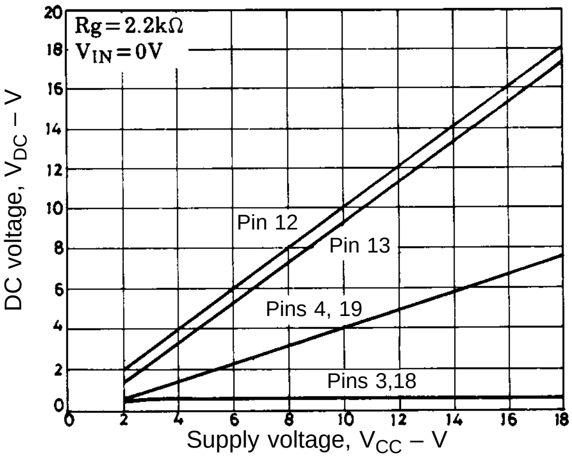
Iccs, Icco – V_{CC}



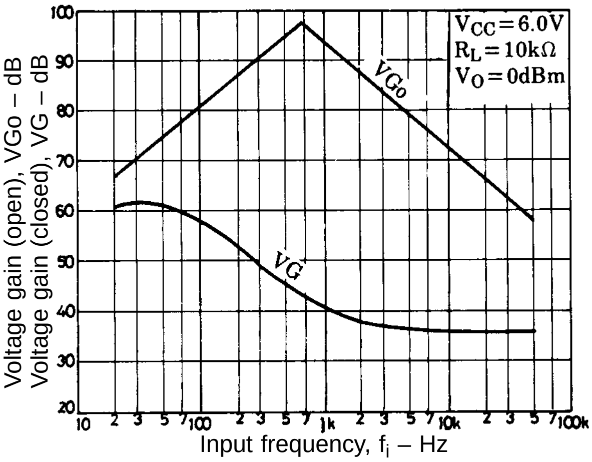
I_B – V_{CC}



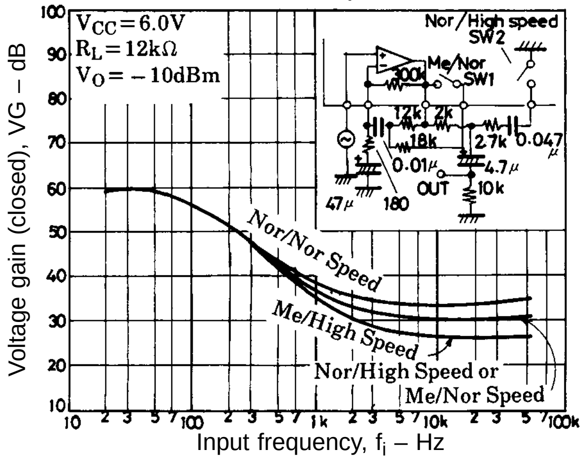
V_{DC} – V_{CC}



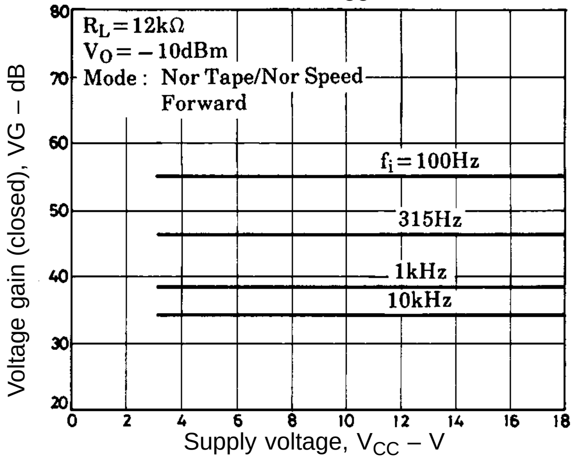
VGo, VG – f_i



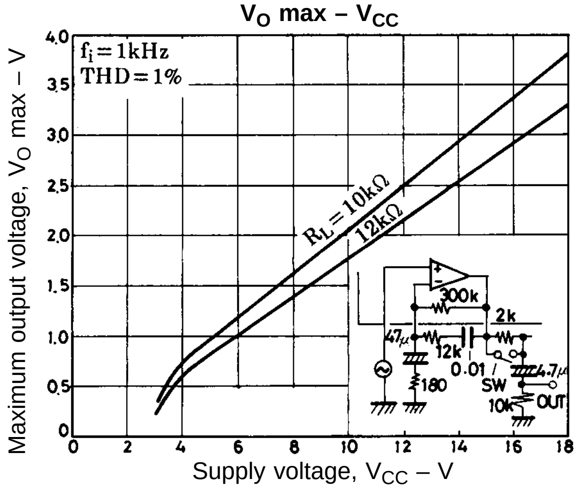
VG – f_i



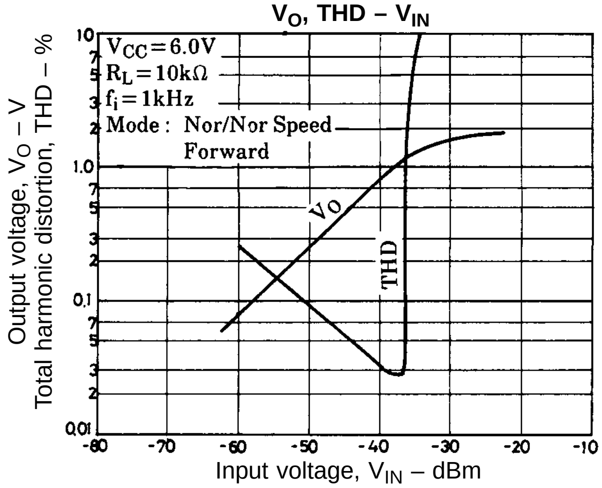
VG – V_{CC}



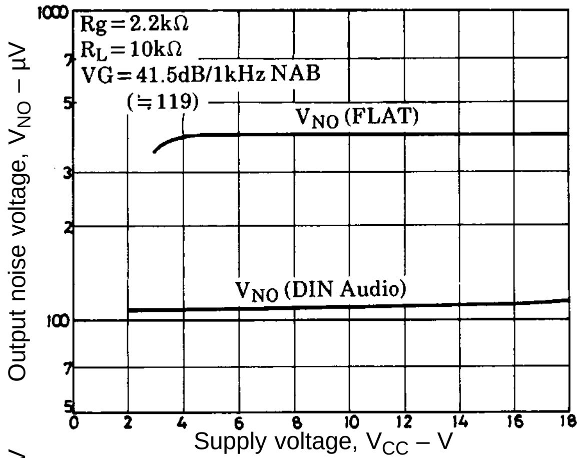
V_O max – V_{CC}



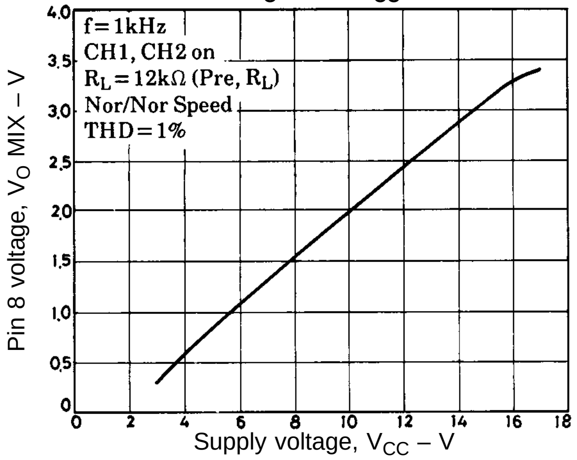
V_O, THD – V_{IN}



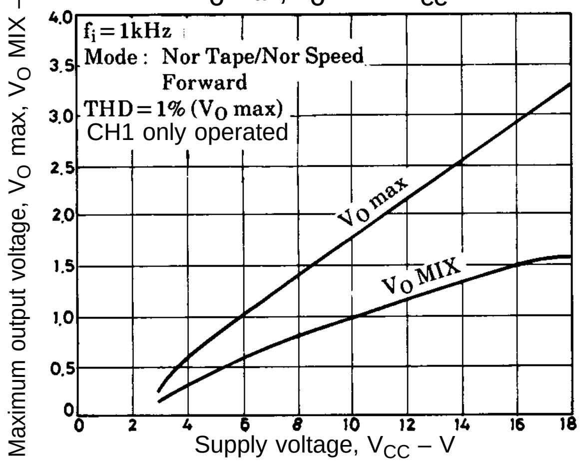
V_{NO} – V_{CC}



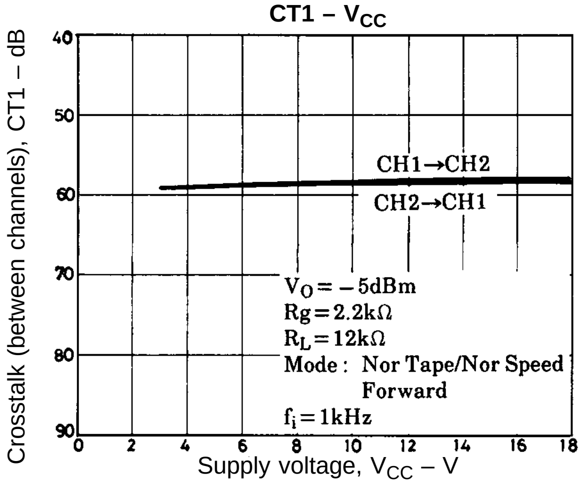
V_O MIX – V_{CC}



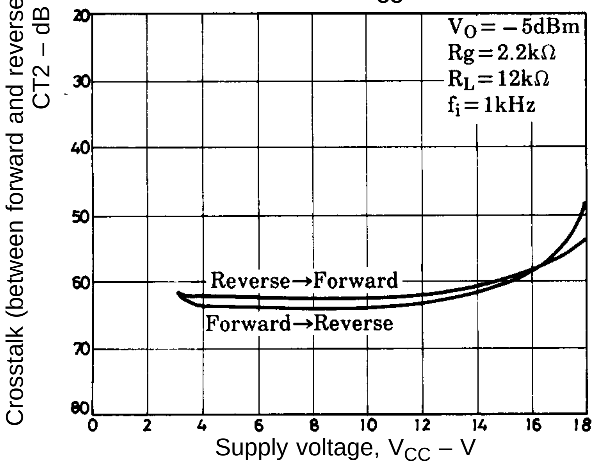
V_O max, V_O MIX – V_{CC}



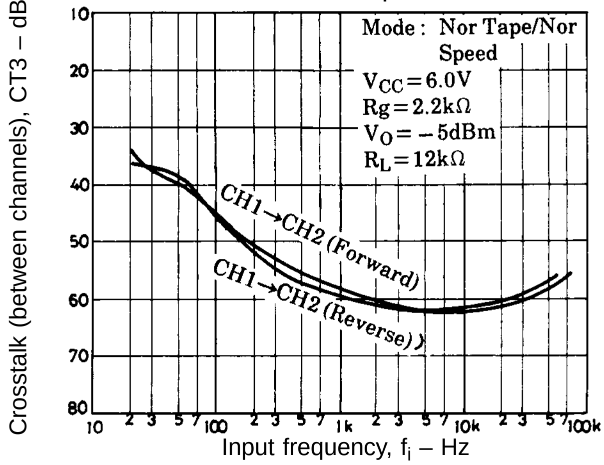
CT1 – V_{CC}



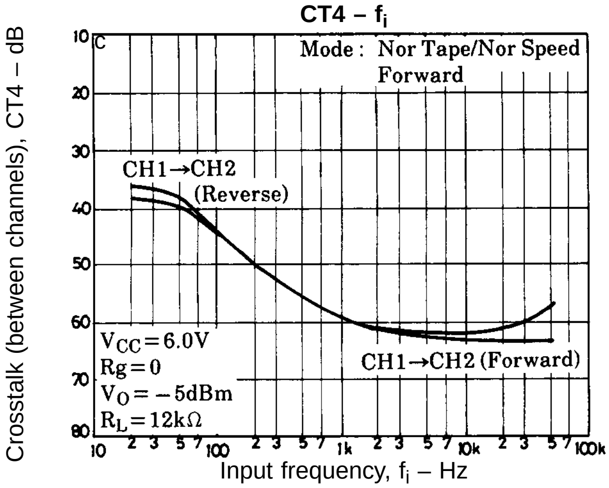
CT2 – V_{CC}



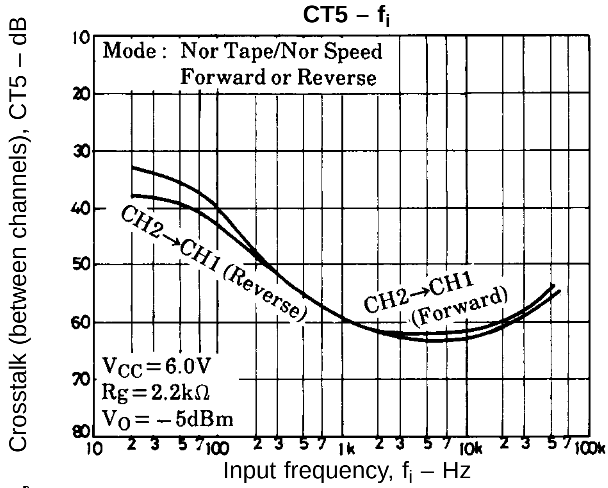
CT3 – f_i



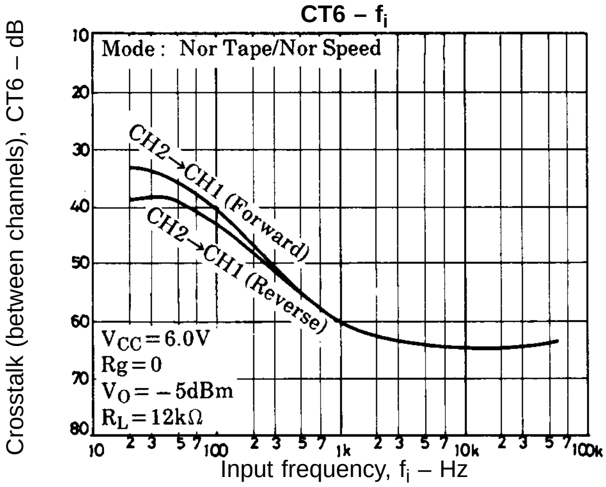
CT4 – f_i



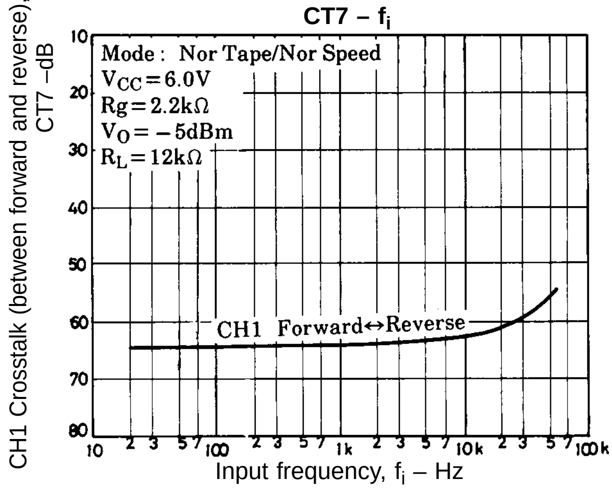
CT5 – f_i



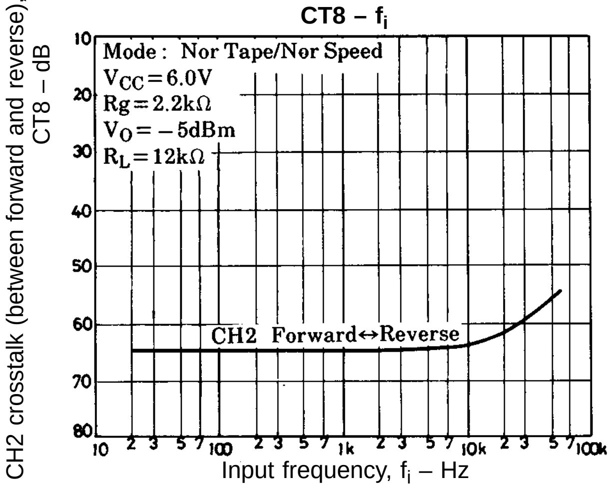
CT6 – f_i



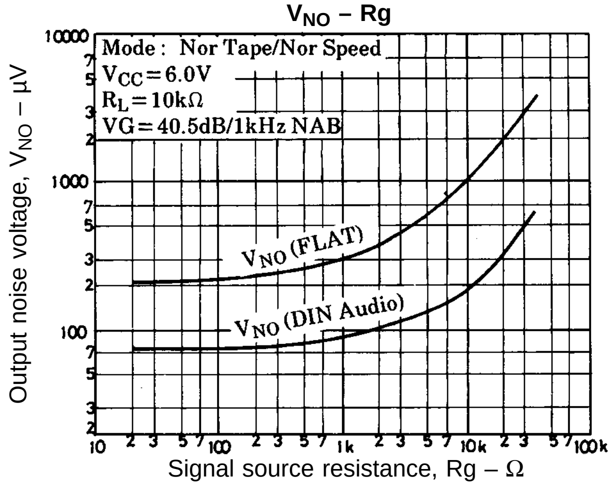
CT7 – f_i



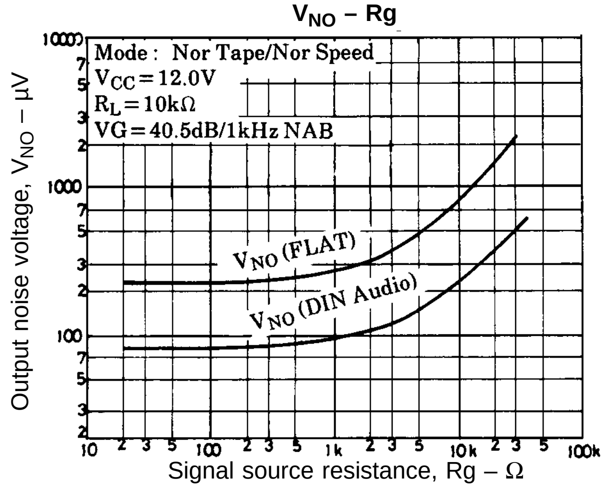
CT8 – f_i



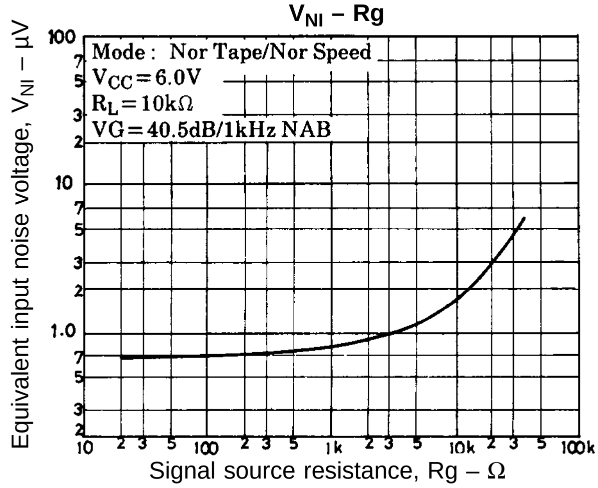
V_{NO} – Rg



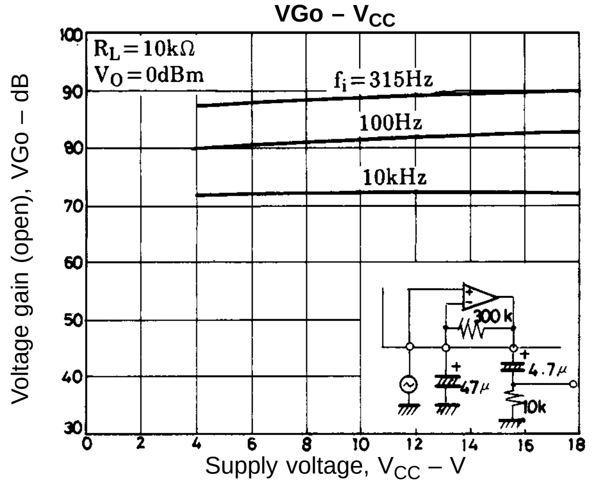
V_{NO} – Rg



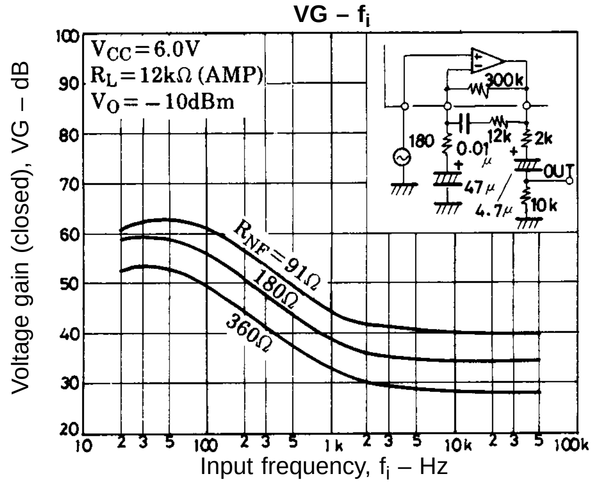
V_{NI} – Rg



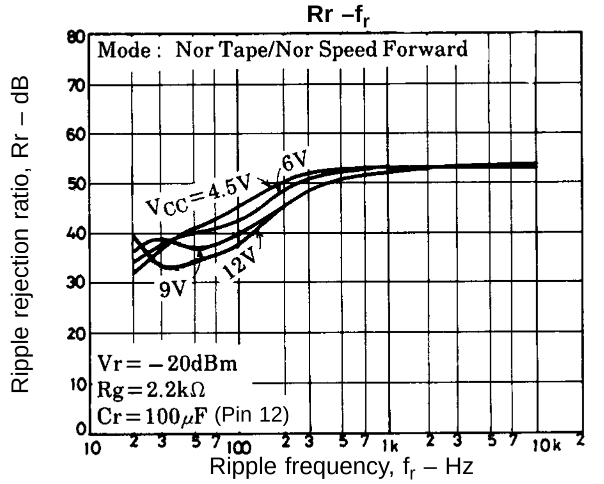
VGo – V_{CC}



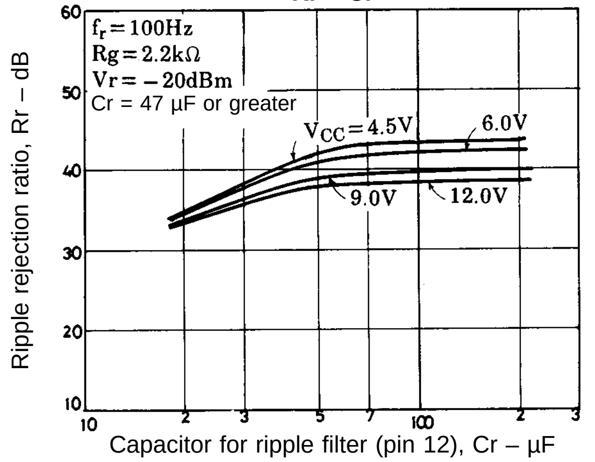
VG – f_i



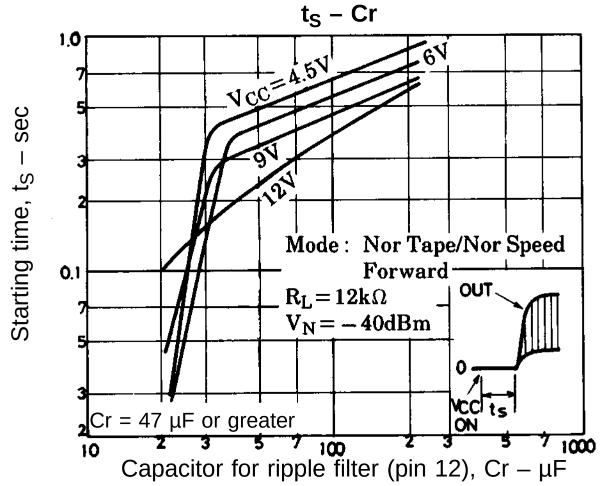
Rr – f_r



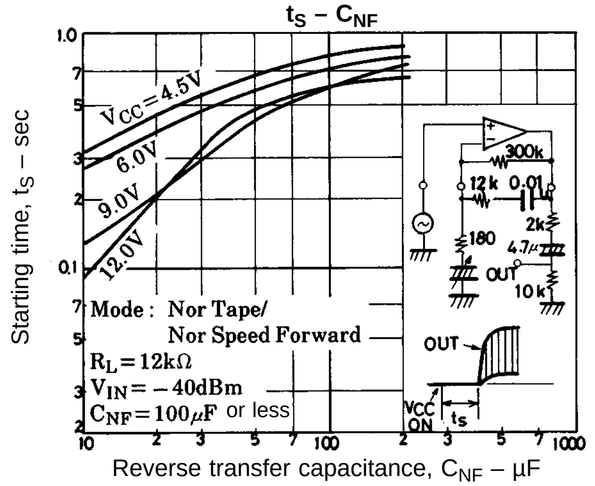
Rr – Cr

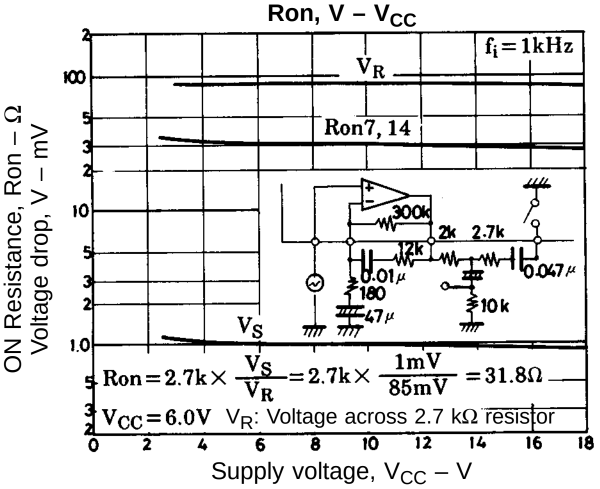


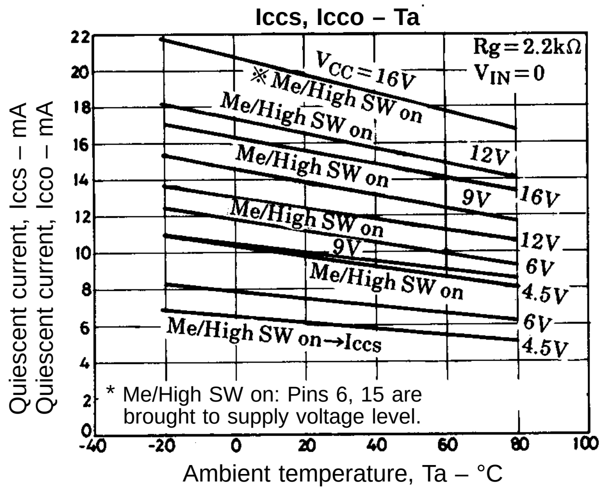
t_S – Cr

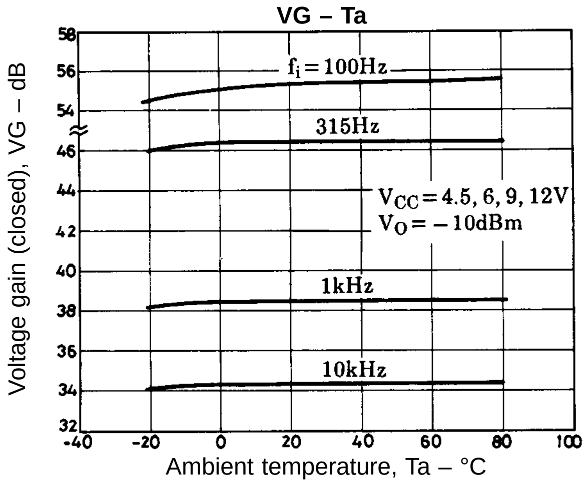


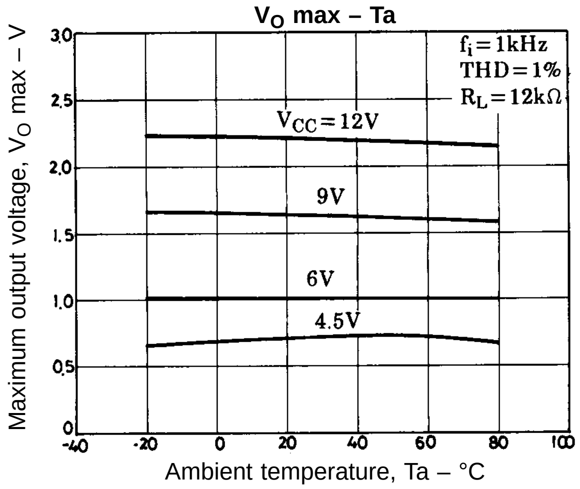
t_S – C_{NF}

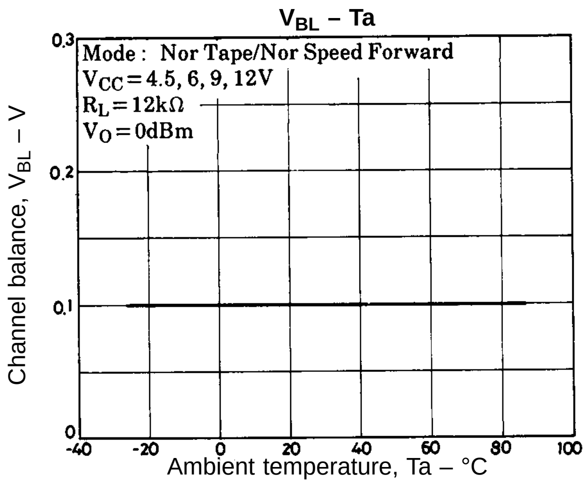


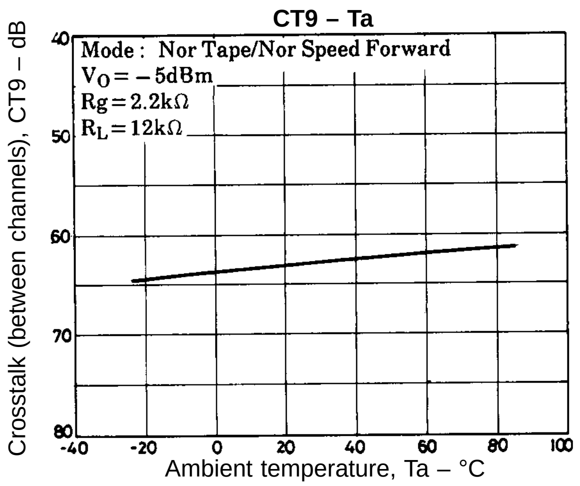

Ron, V – VCC
fi=1kHz
VR
Ron7, 14
VS
Ron=2.7k× VS/VR =2.7k× 1mV/85mV =31.8Ω
VCC=6.0V VR: Voltage across 2.7 kΩ resistor
ON Resistance, Ron – Ω
Voltage drop, V – mV
Supply voltage, VCC – V

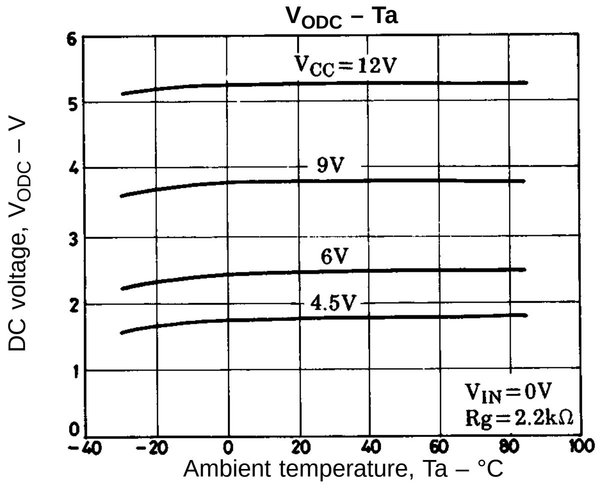

Iccs, Icco – Ta
Rg=2.2kΩ
VIN=0
VCC=16V
※Me/High SW on
Me/High SW on
12V
Me/High SW on
9V
16V
Me/High SW on
12V
9V
6V
Me/High SW on
4.5V
6V
Me/High SW on→Iccs
4.5V
* Me/High SW on: Pins 6, 15 are brought to supply voltage level.
Quiescent current, Iccs – mA
Quiescent current, Icco – mA
Ambient temperature, Ta – °C

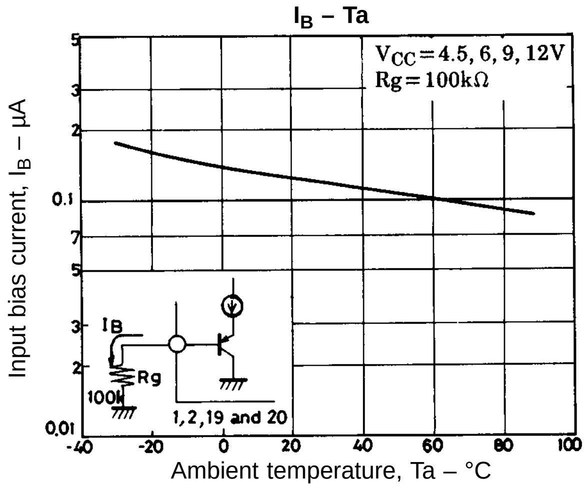

VG – Ta
fi=100Hz
315Hz
VCC=4.5, 6, 9, 12V
VO=–10dBm
1kHz
10kHz
Voltage gain (closed), VG – dB
Ambient temperature, Ta – °C


VO max – Ta
fi=1kHz
THD=1%
RL=12kΩ
VCC=12V
9V
6V
4.5V
Maximum output voltage, VO max – V
Ambient temperature, Ta – °C


VBL – Ta
Mode: Nor Tape/Nor Speed Forward
VCC=4.5, 6, 9, 12V
RL=12kΩ
VO=0dBm
Channel balance, VBL – V
Ambient temperature, Ta – °C


CT9 – Ta
Mode: Nor Tape/Nor Speed Forward
VO=–5dBm
Rg=2.2kΩ
RL=12kΩ
Crosstalk (between channels), CT9 – dB
Ambient temperature, Ta – °C


VODC – Ta
VCC=12V
9V
6V
4.5V
VIN=0V
Rg=2.2kΩ
DC voltage, VODC – V
Ambient temperature, Ta – °C


IB – Ta
VCC=4.5, 6, 9, 12V
Rg=100kΩ
IB
Rg
100k
1, 2, 19 and 20
Input bias current, IB – µA
Ambient temperature, Ta – °C